FAULT DETERMINING APPARATUS FOR DATA TRANSMISSION SYSTEM

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a fault determining apparatus for a data transmission system in a cyclic operating system and, particularly, to a diagnostic apparatus having an operation tracing memory.

2. Description of the Prior Art

In a conventional apparatus, some control parameters useful for diagnostic activity are registered in advance as trace information and this trace information along with detected faults for the latest few operating cycles is stored in a tracing memory so that it can be used for analyzing the faults. In such a conventional system, a parity error signal representing a faulty result of parity check is not included in the record of the tracing memory.

One major purpose of a parity check is to detect erroneous data occurring in the transmission system. However, in the absence of any parity error signal being stored in the tracing memory, no record of a fault in the data transmission system is obtained, and it is not known whether or not the data being traced is transmitted correctly. Therefore, the reliability of the traced data is unknown.

SUMMARY OF THE INVENTION

The present invention is summarized in a fault determining apparatus for a computerized operating system with a trace memory recording selected transmission and fault status wherein there is included parity checking of transmitted data from a main storage or from an input/output unit to a CPU, and the parity error status is also recording in the trace memory.

It is an object of the present invention to provide a fault determining apparatus for a data transmission system capable of overcoming the foregoing prior art deficiency.

Another object of the present invention is to provide a diagnostic apparatus capable of enhancing the reliability of diagnostic functions through the inclusion of the parity error signal in information being traced.

These and other objects and features of the present invention will become more apparent from the following detailed description taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram showing the diagnostic apparatus embodying the present invention;

FIG. **2** is a block diagram showing in more detail the arrangement shown in FIG. **1**; and

FIGS. **3** and **4** are charts showing examples of record logged by the instrumentation unit shown in FIG. **1**.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The invention will now be described with reference to the drawings.

In FIG. **1**, showing in block form one embodiment of the present invention, the apparatus includes a central processing unit (CPU) **1**, a main storage **2**, an input/output (I/O) unit **3**, a tracing memory **4**, a tracing memory retrieval unit **5**, an instrumentation unit **6**, an address command bus **7**, and a data bus **8**. The CPU **1** makes access to the main storage **2** and I/O unit **3** selectively through the address command bus **7**, so that data is transferred among the CPU **1**, main storage **2** and I/O unit **3** through the data bus **8**. Parity information is appended to data which is transferred through the data bus **8** so that any bit error which occurs during the transfer can be detected. Information being traced is stored along with associated parity information and fault information in the tracing memory **4**. The memorized information is retrieved by the tracing memory retrieval unit **5** and recorded by the instrumentation unit **6**.

FIG. **2** shows in more detail the arrangement of FIG. **1**, and common reference numbers are used for counterparts of both figures. In FIG. **2**, parity check circuit **10** receives data on the data bus **8** and a parity bit provided by either parity generator **23** or **30** and performs a parity check on the data transferred on bus **8**. The output of the parity check circuit **10** is connected to the CPU **1** by an interrupt controller **12** which issues an interrupt request to the CPU **1** upon the occurrence of a parity error.

The above-mentioned main storage **2** is made up of ROM **21**, RAM **22** and parity generator **23**. The above-mentioned I/O unit **3** is made up of photocouplers **31***a* and **31***b* for providing electrical isolation to the respective input and output signals, a buffer input register **32**, input and output latches **33***a* and **33***b* for holding data in accordance with signals on the address command bus **7**, and the parity generator **30**. The I/O unit **3** operates to send out information through the output latch **33***b* and photocoupler **31***b* receive information through the input photocoupler **31***a* and latch **33***b*.

The tracing memory **4** is made up of a memory **41** for storing tracing data, a binary counter **42** for generating part by of the address input, such as the more significant bits, for the memory **41** and an address converter **43** which receives signals on the address command bus **7** to generate the remaining part Bx of the address input, such as the lesser significant bits for the tracing memory **41** in correspondence with the successive detection of predetermined address signals on bus **7**, and also to generate a pulse for advancing the count of the counter **42** upon the completion of a cycle.

The tracing memory retrieval unit **5** includes a switch **51** used to set an address corresponding to one of the predetermined source addresses of data recorded in the tracing memory, an address comparator **52** which detects the coincidence of the address signal on the address command bus **7** with the setup of the address setting switch **51**, a latch **53** which holds data on the data bus **8** in response to the address coincidence signal provided by the address comparator **52**, and a D/A converter **54** which converts data held in the latch **53** into an analog signal. The latch **53** also outputs its contents in multi-bit form as shown by **55**. The instrumentation unit **6** operates to record the analog signal provided by the D/A converter **54** or the digital signal provided by the latch **53** directly from the tracing memory retrieval unit **5** over data bus **8**.

The operation of the embodiment will be described in detail. When the CPU **1** makes access to the main storage **2** for reading data, the parity generator **23** within the main storage **2** fetches data on the data bus **8**, generates a parity bit of the even or odd parity mode, and appends the parity signal to a parity bit line **14** of the data bus **8**, and then the stored data with a parity signal